

Equivalence Checking of Digital Circuits

Fundamentals, Principles, Methods

by
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Equivalence Checking Of Digital Circuits Fundamentals Principles Methods

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Equivalence Checking Of Digital Circuits Fundamentals Principles Methods:

Equivalence Checking of Digital Circuits Paul Molitor,Janett Mohnke,2007-05-08 Hardware verification is the process of checking whether a design conforms to its specifications of functionality and timing In today's design processes it becomes more and more important Very large scale integrated VLSI circuits and the resulting digital systems have conquered a place in almost all areas of our life even in security sensitive applications Complex digital systems control airplanes have been used in banks and on intensive care units Hence the demand for error free designs is more important than ever In addition economic reasons underline this demand as well The design and production process of present day VLSI circuits is highly time and cost intensive Moreover it is nearly impossible to repair integrated circuits Thus it is desirable to detect design errors early in the design process and not just after producing the prototype chip All these facts are reflected by developing and production statistics of present day companies For example In neon Technologies 118 assumed that about 60% to 80% of the overall design time was spent for verification in 2000 Other sources cite the 3 to 1 head count ratio between verification engineers and logic designers This shows that verifying logical correctness of the design of hardware systems is a major gate to the problem of time to market of 113 With the chip complexity constantly increasing the difficulty as well as the importance of functional verification of new product designs has been increased It is not only more important to get error free designs

Versatile Hardware Analysis Techniques Lucas Klemmer,Daniel Große,2025-03-06 This book describes several versatile hardware analysis techniques that tackle existing and new challenges These techniques cover different phases of the hardware development process including the verification debugging and post synthesis optimization phases The authors introduce the Waveform Analysis Language WAL which allows users to code analysis tasks in the form of programs that run on waveforms The book covers processor verification formal microcode verification programmable automated waveform analysis demonstrated for a large variety of previously manual analysis tasks as well as netlist optimization leveraging formal methods All methods are available as open source typically include examples on RISC V analysis problems providing a strong foundation for the community

Computer Aided Verification Ruzica Piskac,Zvonimir Rakamarić,2025-07-22 This open access 4 volume set constitutes the proceedings of the 37th International Conference on Computer Aided Verification CAV 2025 held in Zagreb Croatia in July 23 25 2025 The 51 regular papers presented together 24 tool papers 4 case study papers in these proceedings were carefully reviewed and selected from 305 submissions The accepted papers cover a wide spectrum of topics from theoretical results to applications of formal methods These papers apply or extend formal methods to a wide range of domains such as concurrency machine learning and neural networks quantum systems as well as hybrid and stochastic systems

Parallel Computational Technologies Leonid Sokolinsky,Mikhail Zymbler,2023-07-24 This book constitutes the refereed post proceedings of the 17th International Conference on Parallel Computational Technologies PCT 2023 held in Saint Petersburg Russia during March 28 30 2023 The 25 full papers included in this book were carefully

reviewed and selected from 71 submissions They were organized in topical sections as follows High Performance Architectures Tools and Technologies Parallel Numerical Algorithms and Supercomputer Simulation **Books In Print 2004-2005** Ed Bowker Staff,Staff Bowker, Ed,2004 **The British National Bibliography** Arthur James Wells,2004 Courses Catalog - University of Illinois at Urbana-Champaign University of Illinois at Urbana-Champaign,1996 Includes undergraduate and graduate courses **General Catalog -- University of California, Santa Cruz** University of California, Santa Cruz,1993 **Digital System Verification** Lun Li,Mitchell Aaron Thornton,2010 Integrated circuit capacity follows Moore s law and chips are commonly produced at the time of this writing with over 70 million gates per device Ensuring correct functional behavior of such large designs before fabrication poses an extremely challenging problem Formal verification validates the correctness of the implementation of a design with respect to its specification through mathematical proof techniques Formal techniques have been emerging as commercialized EDA tools in the past decade Simulation remains a predominantly used tool to validate a design in industry After more than 50 years of development simulation methods have reached a degree of maturity however new advances continue to be developed in the area A simulation approach for functional verification can theoretically validate all possible behaviors of a design but requires excessive computational resources Rapidly evolving markets demand short design cycles while the increasing complexity of a design causes simulation approaches to provide less and less coverage Formal verification is an attractive alternative since 100% coverage can be achieved however large designs impose unrealistic computational requirements Combining formal verification and simulation into a single integrated circuit validation framework is an attractive alternative This book focuses on an Integrated Design Validation IDV system that provides a framework for design validation and takes advantage of current technology in the areas of simulation and formal verification resulting in a practical validation engine with reasonable runtime After surveying the basic principles of formal verification and simulation this book describes the IDV approach to integrated circuit functional validation *General Catalogue* Santa Barbara State Teachers College,1976 International Aerospace Abstracts ,1989 **University of Colorado at Colorado Springs Bulletin** University of Colorado at Colorado Springs,1994 *Documentation Abstracts* ,1987 Formal Equivalence Checking and Design Debugging Shi-Yu Huang,Kwang-Ting (Tim) Cheng,2012-12-06 Formal Equivalence Checking and Design Debugging covers two major topics in design verification logic equivalence checking and design debugging The first part of the book reviews the design problems that require logic equivalence checking and describes the underlying technologies that are used to solve them Some novel approaches to the problems of verifying design revisions after intensive sequential transformations such as retiming are described in detail The second part of the book gives a thorough survey of previous and recent literature on design error diagnosis and design error correction This part also provides an in depth analysis of the algorithms used in two logic debugging software programs ErrorTracer and AutoFix developed by the authors From the Foreword With the adoption

of the static sign off approach to verifying circuit implementations the application specific integrated circuit ASIC industry will experience the first radical methodological revolution since the adoption of logic synthesis Equivalence checking is one of the two critical elements of this methodological revolution This book is timely for either the designer seeking to better understand the mechanics of equivalence checking or for the CAD researcher who wishes to investigate well motivated research problems such as equivalence checking of retimed designs or error diagnosis in sequential circuits Kurt Keutzer University of California Berkeley

Catalogs of Courses University of California, Berkeley,1995 Includes general and summer catalogs issued between 1878 1879 and 1995 1997

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