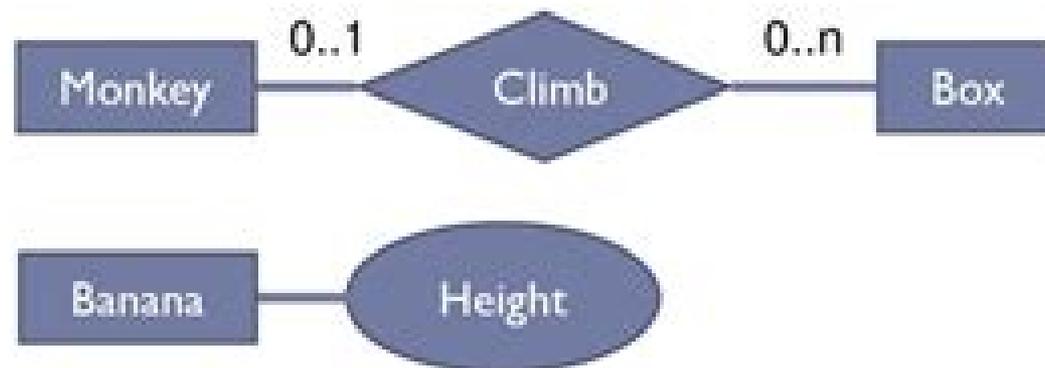


Languages with formal syntax

- In the **Entity-Relationship (ER) Model** [Chen 1976] the alphabet is a set of graphical objects, that are used to construct schemas (the sentences).



- Examples of ER sentences:



Formal Syntax

Henry Sweet



Formal Syntax:

Formal Syntax Peter W. Culicover, Thomas Wasow, Adrian Akmajian, 1977 The Verilog® Hardware Description Language Donald Thomas, Philip Moorby, 2008-09-11 xv From the Old to the New xvii Acknowledgments xx Verilog A Tutorial Introduction Getting Started 2 A Structural Description 2 Simulating the binaryToESeg Driver 4 Creating Ports For the Module 7 Creating a Testbench For a Module 8 Behavioral Modeling of Combinational Circuits 11 Procedural Models 12 Rules for Synthesizing Combinational Circuits 13 Procedural Modeling of Clocked Sequential Circuits 14 Modeling Finite State Machines 15 Rules for Synthesizing Sequential Systems 18 Non Blocking Assignment **Dictionary of Logic as Applied in the Study of Language** W. Marciszewski, 2013-06-29 1 STRUCTURE AND REFERENCES 1 1 The main part of the dictionary consists of alphabetically arranged articles concerned with basic logical theories and some other selected topics Within each article a set of concepts is defined in their mutual relations This way of defining concepts in the context of a theory provides better understanding of ideas than that provided by isolated short definitions A disadvantage of this method is that it takes more time to look something up inside an extensive article To reduce this disadvantage the following measures have been adopted Each article is divided into numbered sections the numbers in boldface type being addresses to which we refer Those sections of larger articles which are divided at the first level i e numbered with single numerals have titles Main sections are further subdivided the subsections being numbered by numerals added to the main section number e g I 1 1 2 1 1 1 1 2 and so on A comprehensive subject index is supplied together with a glossary The aim of the latter is to provide if possible short definitions which sometimes may prove sufficient As to the use of the glossary see the comment preceding it **The Verilog® Hardware Description Language** Donald E. Thomas, Philip R. Moorby, 2013-04-18 xvii Acknowledgments CHAPTER 1 Verilog A Tutorial Introduction 1 Getting Started 2 A Structural Description 2 Simulating the NAND Latch 4 Module Hleral Chy 6 The Counter 7 Components of the Counter 9 A Clock for the System 10 Tying the Whole Circuit Together 11 Using An Alternate Description of the Flip Flop 13 Behavioral Modeling 1 S A Behavioral Model of the m16 Counter 16 Mixing Structure and Behavior 18 Assignment Statements 22 Summary on Mixing Behavioral and Structural Descriptions 23 Creating a Testbench For a Module 24 Summary 2S Tutorial Guide to Formal Syntax Specification 26 Exercises 30 CHAPTER 2 Behavioral Modeling 33 Process Model 33 If Then Else 3S Where Does The ELSE Belong 39 The Conditional Operator 41 Loops 41 Four Basic Loop Statements 42 Exiting Loops on Exceptional Conditions 45 Multi way branching 46 If Else If 46 Case 46 Comparison of Case and If Else If 48 viii The Verilog Hardware Description Language Casez and Casex 49 Functions and Tasks SO Tasks 52 Functions 55 A Structural View 57 Rules of Scope and Hierarchical Names S9 Rules of Scope 60 Hierarchical Names 62 Summary 63 Exerdses 63 CHAPTER 3 Concurrent Processes 6S Concuent Processes 6S Events 67 Event Control Statement 67 Named Events 69 The Wait Statement 72 A Complete Producer Consumer Handshake 74 Comparison of the Wait and While Statements 77 Comparison of Wait and Event Control

Statements 78 A Concurrent Process Example 78 Disabling Named Blocks 84 Intra Assignment Control and Timing Events 87
 Procedural Continuous Assignment 90 **The practical study of languages, a guide** Henry Sweet,1899 A manual of
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