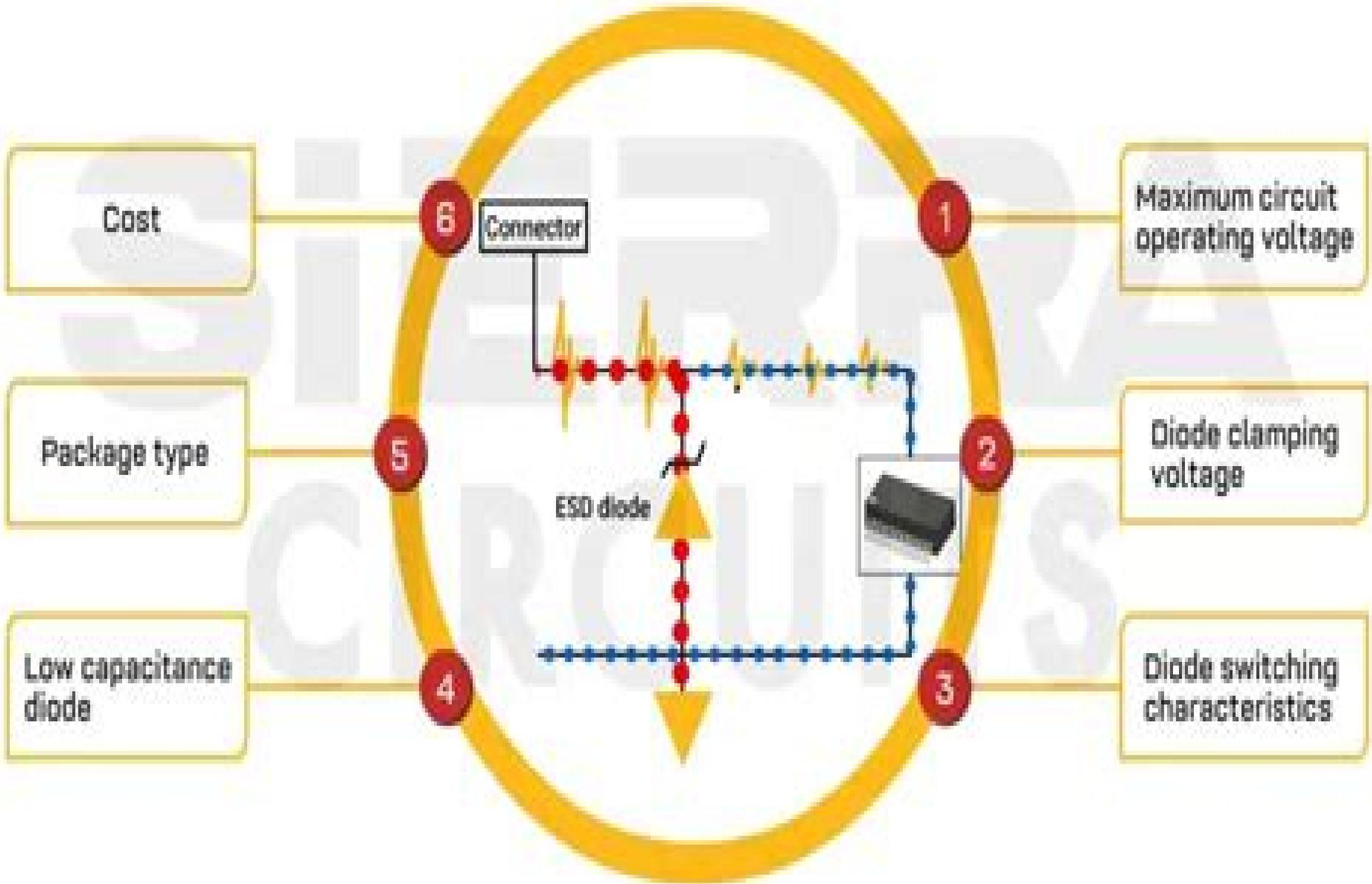


Factors to consider when selecting an ESD diode



Esd Circuits And Systems

S Marginson



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ESD Steven H. Voldman, 2015-04-24 *ESD Circuits and Devices* 2nd Edition provides a clear picture of layout and design of digital analog radio frequency RF and power applications for protection from electrostatic discharge ESD electrical overstress EOS and latchup phenomena from a generalist perspective and design synthesis practices providing optimum solutions in advanced technologies New features in the 2nd edition Expanded treatment of ESD and analog design of passive devices of resistors capacitors inductors and active devices of diodes bipolar junction transistors MOSFETs and FINFETs Increased focus on ESD power clamps for power rails for CMOS Bipolar and BiCMOS Co synthesizing of semiconductor chip architecture and floor planning with ESD design practices for analog and mixed signal applications Illustrates the influence of analog design practices on ESD design circuitry from integration synthesis and layout to symmetry matching inter digitation and common centroid techniques Increased emphasis on system level testing conforming to IEC 61000 4 2 and IEC 61000 4 5 Improved coverage of low capacitance ESD scaling of devices and oxide scaling challenges *ESD Circuits and Devices* 2nd Edition is an essential reference to ESD circuit semiconductor engineers and quality reliability analysis engineers It is also useful for graduate and undergraduate students in electrical engineering semiconductor sciences microelectronics and IC design

ESD Steven H. Voldman, 2011-04-04 *Electrostatic discharge ESD* continues to impact semiconductor components and systems as technologies scale from micro to nano electronics This book studies electrical overstress ESD and latchup from a whole chip ESD design synthesis approach It provides a clear insight into the integration of ESD protection networks from a generalist perspective followed by examples in specific technologies circuits and chips Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks are covered from a top down design approach Look inside for extensive coverage on integration of cores power bussing and signal pins in DRAM SRAM CMOS image processing chips microprocessors analog products RF components and how the integration influences ESD design and integration architecturing of mixed voltage mixed signal to RF design for ESD analysis floorplanning for peripheral and core I O designs and the implications on ESD and latchup guard ring integration for both a bottom up and top down methodology addressing I O guard rings ESD guard rings I O to I O and I O to core classification of ESD power clamps and ESD signal pin circuitry and how to make the correct choice for a given semiconductor chip examples of ESD design for the state of the art technologies discussed including CMOS BiCMOS silicon on insulator SOI bipolar technology high voltage CMOS HVCMOS RF CMOS and smart power practical methods for the understanding of ESD circuit power distribution ground rule development internal bus distribution current path analysis quality metrics *ESD Design and Synthesis* is a continuation of the author s series of books on ESD protection It is an essential reference for ESD circuit and semiconductor engineers design synthesis team leaders layout design characterisation floorplanning test and reliability engineers technicians and groundrule and test site developers in the manufacturing and design of semiconductor chips It is also useful

for graduate and undergraduate students in electrical engineering semiconductor sciences and manufacturing sciences and on courses involving the design of ESD devices chips and systems This book offers a useful insight into the issues that confront modern technology as we enter the nano electronic era [ESD](#) Steven H. Voldman,2006-11-02 With the growth of high speed telecommunications and wireless technology it is becoming increasingly important for engineers to understand radio frequency RF applications and their sensitivity to electrostatic discharge ESD phenomena This enables the development of ESD design methods for RF technology leading to increased protection against electrical overstress EOS and ESD ESD RF Technology and Circuits Presents methods for co synthesizing ESD networks for RF applications to achieve improved performance and ESD protection of semiconductor chips discusses RF ESD design methods of capacitance load transformation matching network co synthesis capacitance shunts inductive shunts impedance isolation load cancellation methods distributed loads emitter degeneration buffering and ballasting examines ESD protection and design of active and passive elements in RF complementary metal oxide semiconductor CMOS RF laterally diffused metal oxide semiconductor LDMOS RF BiCMOS Silicon Germanium SiGe RF BiCMOS Silicon Germanium Carbon SiGeC and Gallium Arsenide technology gives information on RF ESD testing methodologies RF degradation effects and failure mechanisms for devices circuits and systems highlights RF ESD mixed signal design integration of digital analog and RF circuitry sets out examples of RF ESD design computer aided design methodologies covers state of the art RF ESD input circuits as well as voltage triggered to RC triggered ESD power clamps networks in RF technologies as well as off chip protection concepts Following the authors series of books on ESD this book will be a thorough overview of ESD in RF technology for RF semiconductor chip and ESD engineers Device and circuit engineers working in the RF domain and quality reliability and failure analysis engineers will also find it a valuable reference in the rapidly growing area of RF ESD design In addition it will appeal to graduate students in RF microwave technology and RF circuit design [The ESD Handbook](#) Steven H. Voldman,2021-03-25 A practical and comprehensive reference that explores Electrostatic Discharge ESD in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection Written by a noted expert on the topic the text offers a topic by topic reference that includes illustrative figures discussions and drawings The handbook covers a wide range of topics including ESD in manufacturing garments wrist straps and shoes ESD Testing ESD device physics ESD semiconductor process effects ESD failure mechanisms ESD circuits in different technologies CMOS Bipolar etc ESD circuit types Pin Power Pin to Pin etc and much more In addition the text includes a glossary index tables illustrations and a variety of case studies Contains a well organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications

Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians operators engineers circuit designers and failure analysis engineers The ESD Handbook contains an accessible reference to ESD design and ESD systems

System Level ESD Protection Vladislav Vashchenko, Mirko Scholz, 2014-03-21 This book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge ESD protection It is an invaluable reference for anyone developing systems on chip SoC and systems on package SoP integrated with system level ESD protection The book focuses on both the design of semiconductor integrated circuit IC components with embedded on chip system level protection and IC system co design The readers will be enabled to bring the system level ESD protection solutions to the level of integrated circuits thereby reducing or completely eliminating the need for additional discrete components on the printed circuit board PCB and meeting system level ESD requirements The authors take a systematic approach based on IC system ESD protection co design A detailed description of the available IC level ESD testing methods is provided together with a discussion of the correlation between IC level and system level ESD testing methods The IC level ESD protection design is demonstrated with representative case studies which are analyzed with various numerical simulations and ESD testing The overall methodology for IC system ESD co design is presented as a step by step procedure that involves both ESD testing and numerical simulations

ESD Steven H. Voldman, 2015-01-05 A comprehensive and in depth review of analog circuit layout schematic architecture device power network and ESD design This book will provide a balanced overview of analog circuit design layout analog circuit schematic development architecture of chips and ESD design It will start at an introductory level and will bring the reader right up to the state of the art Two critical design aspects for analog and power integrated circuits are combined The first design aspect covers analog circuit design techniques to achieve the desired circuit performance The second and main aspect presents the additional challenges associated with the design of adequate and effective ESD protection elements and schemes A comprehensive list of practical application examples is used to demonstrate the successful combination of both techniques and any potential design trade offs Chapter One looks at analog design discipline including layout and analog matching and analog layout design practices Chapter Two discusses analog design with circuits examining single transistor amplifiers multi transistor amplifiers active loads and more The third chapter covers analog design layout also MOSFET layout before Chapters Four and Five discuss analog design synthesis The next chapters introduce the reader to analog digital mixed signal design synthesis analog signal pin ESD networks and analog ESD power clamps Chapter Nine the last chapter covers ESD design in analog applications Clearly describes analog design fundamentals circuit fundamentals as well as outlining the various ESD implications Covers a large breadth of subjects and technologies such as CMOS LDMOS BCD SOI and thick body SOI Establishes an ESD analog design discipline that distinguishes itself from the alternative ESD digital design focus Focuses on circuit and circuit design applications Assessible with the artwork and tutorial style of the ESD book series

PowerPoint slides are available for university faculty members Even in the world of digital circuits analog and power circuits are two very important but under addressed topics especially from the ESD aspect Dr Voldman s new book will serve as an essential and practical guide to the greater IC community With high practical and academic values this book is a bible for professionals graduate students device and circuit designers for investigating the physics of ESD and for product designs and testing

ESD Testing Steven H. Voldman,2016-10-07 With the evolution of semiconductor technology and global diversification of the semiconductor business testing of semiconductor devices to systems for electrostatic discharge ESD and electrical overstress EOS has increased in importance ESD Testing From Components to Systems updates the reader in the new tests test models and techniques in the characterization of semiconductor components for ESD EOS and latchup Key features Provides understanding and knowledge of ESD models and specifications including human body model HBM machine model MM charged device model CDM charged board model CBM cable discharge events CDE human metal model HMM IEC 61000 4 2 and IEC 61000 4 5 Discusses new testing methodologies such as transmission line pulse TLP to very fast transmission line pulse VF TLP and future methods of long pulse TLP to ultra fast TLP UF TLP Describes both conventional testing and new testing techniques for both chip and system level evaluation Addresses EOS testing electromagnetic compatibility EMC scanning to current reconstruction methods Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing ESD Testing From Components to Systems is part of the authors series of books on electrostatic discharge ESD protection this book will be an invaluable reference for the professional semiconductor chip and system level ESD and EOS test engineer Semiconductor device and process development circuit designers quality reliability and failure analysis engineers will also find it an essential reference In addition its academic treatment will appeal to both senior and graduate students with interests in semiconductor process device physics semiconductor testing and experimental work

Electrostatic Discharge Protection Juin J. Liou,2017-07-26 Electrostatic discharge ESD is one of the most prevalent threats to electronic components In an ESD event a finite amount of charge is transferred from one object i e human body to another i e microchip This process can result in a very high current passing through the microchip within a very short period of time Thus more than 35 percent of single event chip damages can be attributed to ESD events and designing ESD structures to protect integrated circuits against the ESD stresses is a high priority in the semiconductor industry Electrostatic Discharge Protection Advances and Applications delivers timely coverage of component and system level ESD protection for semiconductor devices and integrated circuits Bringing together contributions from internationally respected researchers and engineers with expertise in ESD design optimization modeling simulation and characterization this book bridges the gap between theory and practice to offer valuable insight into the state of the art of ESD protection Amply illustrated with tables figures and case studies the text Instills a deeper understanding of ESD events and ESD protection design principles Examines vital processes including Si CMOS Si BCD Si SOI and GaN

technologies Addresses important aspects pertinent to the modeling and simulation of ESD protection solutions Electrostatic Discharge Protection Advances and Applications provides a single source for cutting edge information vital to the research and development of effective robust ESD protection solutions for semiconductor devices and integrated circuits ESD Protection Methodologies Marise Bafleur, Fabrice Caignet, Nicolas Nolhier, 2017-07-26 Failures caused by electrostatic discharges ESD constitute a major problem concerning the reliability and robustness of integrated circuits and electronic systems This book summarizes the many diverse methodologies aimed at ESD protection and shows through a number of concrete studies that the best approach in terms of robustness and cost effectiveness consists of implementing a global strategy of ESD protection ESD Protection Methodologies begins by exploring the various normalized test techniques that are used to qualify ESD robustness as well as characterization and defect localization methods aimed at implementing corrective measures Due to the increasing complexity of integrated circuits it is important to be able to provide a simulation in which the implemented ESD protection strategy provides the desired protection while not harming the performance levels of the circuit Therefore the main features and difficulties related to the different types of simulation finite element SPICE type and behavioral are then studied To conclude several case studies are presented which provide real life examples of the approaches explained in the previous chapters and validate a number of the strategies from component to system level Provides a global ESD protection approach from component to system including both the proposal of investigation techniques and predictive simulation methodologies Addresses circuit and system designers as well as failure analysis engineers Provides the description of specifically developed investigation techniques and the application of the proposed methodologies to real case studies **ESD** Steven H. Voldman, 2009-07-01 Electrostatic discharge ESD failure mechanisms continue to impact semiconductor components and systems as technologies scale from micro to nano electronics This book studies electrical overstress ESD and latchup from a failure analysis and case study approach It provides a clear insight into the physics of failure from a generalist perspective followed by investigation of failure mechanisms in specific technologies circuits and systems The book is unique in covering both the failure mechanism and the practical solutions to fix the problem from either a technology or circuit methodology Look inside for extensive coverage on failure analysis tools EOS and ESD failure sources and failure models of semiconductor technology and how to use failure analysis to design more robust semiconductor components and systems electro thermal models and technologies the state of the art technologies discussed include CMOS BiCMOS silicon on insulator SOI bipolar technology high voltage CMOS HVCMOS RF CMOS smart power gallium arsenide GaAs gallium nitride GaN magneto resistive MR giant magneto resistors GMR tunneling magneto resistor TMR devices micro electro mechanical MEM systems and photo masks and reticles practical methods to use failure analysis for the understanding of ESD circuit operation temperature analysis power distribution ground rule development internal bus distribution current path analysis quality metrics connecting the theoretical to the practical analysis the failure of each key

element of a technology from passives active elements to the circuit sub system to package highlighted by case studies of the elements circuits and system on chip SOC in today s products ESD Failure Mechanisms and Models is a continuation of the author s series of books on ESD protection It is an essential reference and a useful insight into the issues that confront modern technology as we enter the Nano electronic era **Electrical Overstress (EOS)** Steven H. Voldman,2013-08-27

Electrical Overstress EOS continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano electronics This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures The text provides a clear picture of EOS phenomena EOS origins EOS sources EOS physics EOS failure mechanisms and EOS on chip and system design It provides an illuminating insight into the sources of EOS in manufacturing integration of on chip and system level EOS protection networks followed by examples in specific technologies circuits and chips The book is unique in covering the EOS manufacturing issues from on chip design and electronic design automation to factory level EOS program management in today s modern world Look inside for extensive coverage on Fundamentals of electrical overstress from EOS physics EOS time scales safe operating area SOA to physical models for EOS phenomena EOS sources in today s semiconductor manufacturing environment and EOS program management handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices circuits and system Discussion of how to distinguish between EOS events and electrostatic discharge ESD events e g such as human body model HBM charged device model CDM cable discharge events CDM charged board events CBE to system level IEC 61000 4 2 test events EOS protection on chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards PCB and manufacturing equipment Examples of EOS issues in state of the art digital analog and power technologies including CMOS LDMOS and BCD EOS design rule checking DRC LVS and ERC electronic design automation EDA and how it is distinct from ESD EDA systems EOS testing and qualification techniques and Practical off chip ESD protection and system level solutions to provide more robust systems

Electrical Overstress EOS Devices Circuits and Systems is a continuation of the author s series of books on ESD protection It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano electronic era **IEEE Transactions on Circuits and Systems** ,2006 *IEEE International Conference on Electronics, Circuits and Systems* ,1998 *1992 IEEE International Symposium on Circuits and Systems* Stanley A. White,Institute of Electrical and Electronics Engineers,1992 ISCAS 98 provides the latest results on many important subjects in computer aided design modeling and simulation testing signal processing neural and fuzzy systems multimedia image and video processing linear and nonlinear circuits and systems and many more exciting fields *ESD Design for Analog Circuits* Vladislav A. Vashchenko,Andrei Shibkov,2010-07-27 This Book and Simulation Software Bundle Project Dear Reader this book project brings to you a unique study tool for ESD protection solutions used in analog integrated circuit IC design Quick start learning

is combined with in depth understanding for the whole spectrum of cross disciplinary knowledge required to excel in the ESD field. The chapters cover technical material from elementary semiconductor structure and device levels up to complex analog circuit design examples and case studies. The book project provides two different options for learning the material. The printed material can be studied as any regular technical textbook. At the same time another option adds parallel exercise using the trial version of a complementary commercial simulation tool with prepared simulation examples. Combination of the textbook material with numerical simulation experience presents a unique opportunity to gain a level of expertise that is hard to achieve otherwise. The book is bundled with simplified trial version of commercial mixed mode simulation software from Angstrom Design Automation. The DECIMM Device Circuit Mixed Mode simulator tool and complementary to the book's simulation examples can be downloaded from www.analogesd.com. The simulation examples prepared by the authors support the specific examples discussed across the book chapters. A key idea behind this project is to provide an opportunity to not only study the book material but also gain a much deeper understanding of the subject by direct experience through practical simulation examples.

Proceedings of the ... IEEE International Caracas Conference on Devices, Circuits and Systems, 2004 [Understanding, Modeling, and Mitigating System-level ESD in Integrated Circuits](#) Robert M. Mertens, 2015

Practical ESD Protection Design Albert Wang, 2021-12-07 An authoritative single volume reference on the design and analysis of ESD protection for ICs. Electrostatic discharge ESD is a major reliability challenge to semiconductors, integrated circuits, ICs, and microelectronic systems. On-chip ESD protection is a vital to any electronic products such as smartphones, laptops, tablets, and other electronic devices. Practical ESD Protection Design provides comprehensive and systematic guidance on all major aspects of designs of on-chip ESD protection for integrated circuits, ICs. Written for students and practicing engineers alike, this one-stop resource covers essential theories, hands-on design skills, computer-aided design (CAD) methods, characterization, and analysis techniques, and more on ESD protection designs. Detailed chapters examine an array of topics ranging from fundamental to advanced, including ESD phenomena, ESD failure analysis, ESD testing models, ESD protection devices and circuits, ESD design layout and technology effects, ESD design flows, and co-design methods, ESD modelling, and CAD techniques, and future ESD protection concepts. Based on the author's decades of design research and teaching experiences, Practical ESD Protection Design features numerous real-world ESD protection design examples. Emphasizes on ESD protection design techniques and procedures. Describes ESD IC co-design methodology for high performance mixed signal ICs and broadband radio frequency (RF) ICs. Discusses CAD based ESD protection design optimization and prediction using both Technology and Electrical Computer Aided Design (TCAD/ECAD) simulation. Addresses new ESD CAD algorithms and tools for full-chip ESD physical design verification. Explores the disruptive future outlook of ESD protection. Practical ESD Protection Design is a valuable reference for industrial engineers and academic researchers in the field and an excellent textbook for electronic engineering courses in semiconductor, microelectronics, and integrated

circuit designs

System and Component Failure from Electrical Overstress and Electrostatic Discharge Steven H. Voldman, 2018 Electrical overstress EOS and electrostatic discharge ESD have been an issue in devices circuit and systems for electronics for many decades as early as the 1970s and continued to be an issue to today In this chapter the issue of EOS and ESD will be discussed The sources of both EOS and ESD failure history will be discussed EOS and ESD physical models failure mechanisms testing methods and solutions will be shown The chapter will close with discussion on how to provide both EOS and ESD robust devices circuits and systems design practices and procedures as well as EOS and ESD factory control programs EOS sources also occur from design characteristics of devices circuits and systems

ESD Basics Steven H. Voldman, 2012-10-22 Electrostatic discharge ESD continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano electronics This book introduces the fundamentals of ESD electrical overstress EOS electromagnetic interference EMI electromagnetic compatibility EMC and latchup as well as provides a coherent overview of the semiconductor manufacturing environment and the final system assembly It provides an illuminating look into the integration of ESD protection networks followed by examples in specific technologies circuits and chips The text is unique in covering semiconductor chip manufacturing issues ESD semiconductor chip design and system problems confronted today as well as the future of ESD phenomena and nano technology Look inside for extensive coverage on The fundamentals of electrostatics triboelectric charging and how they relate to present day manufacturing environments of micro electronics to nano technology Semiconductor manufacturing handling and auditing processing to avoid ESD failures ESD EOS EMI EMC and latchup semiconductor component and system level testing to demonstrate product resilience from human body model HBM transmission line pulse TLP charged device model CDM human metal model HMM cable discharge events CDE to system level IEC 61000 4 2 tests ESD on chip design and process manufacturing practices and solutions to improve ESD semiconductor chip solutions also practical off chip ESD protection and system level solutions to provide more robust systems System level concerns in servers laptops disk drives cell phones digital cameras hand held devices automobiles and space applications Examples of ESD design for state of the art technologies including CMOS BiCMOS SOI bipolar technology high voltage CMOS HVCMOS RF CMOS smart power magnetic recording technology micro machines MEMs to nano structures ESD Basics From Semiconductor Manufacturing to Product Use complements the author's series of books on ESD protection For those new to the field it is an essential reference and a useful insight into the issues that confront modern technology as we enter the Nano electronic Era

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