

# High-Performance Energy-Efficient Microprocessor Design

*Edited by*  
Vojin G. Oklobdzija and Ram K. Krishnamurthy

# Energy Efficient Microprocessor Design

**Anantha Chandrakasan**



## **Energy Efficient Microprocessor Design:**

*High-Performance Energy-Efficient Microprocessor Design* Vojin G. Oklobdzija, Ram K. Krishnamurthy, 2007-04-27

Microprocessors of today contain close to a billion transistors while achieving the performance of super computers just a decade ago. Designing such processors takes hundreds of people organized into large teams. High Performance Energy Efficient Microprocessor Design is written by the world's most prominent microprocessor design leaders from the industry and academia. It provides a complete coverage of all the aspects of a complex microprocessor design process from technology, power management, clocking, high performance architecture, design methodologies, memory and I/O design, computer aided design, testing and design for testability. The chapters are written to provide the latest state of the art knowledge of particular aspects of microprocessor design while including sufficient tutorial content in order to bring non experts up to speed. High Performance Energy Efficient Microprocessor Design is intended to be a useful companion book for every design engineer working in the related areas and a source of technical information as well as a comprehensive reference in the field. It should also serve as the source book for technical and business managers involved in microprocessor based design and manufacture. The chapters are organized in a way which makes it possible to use this book as a textbook for graduate courses in advanced digital and system design. The book is intended to highlight practical problems encountered in designing state of the art processors while yet covering fundamental principles that are independent of technology.

**Energy Efficient Microprocessor Design** Thomas D. Burd, Robert W. Brodersen, 2012-12-06 This work began in 1995 as an outgrowth of the InfoPad project which showed us that in order to reduce the energy consumption of a portable multimedia terminal that something had to be done about the consumption of the microprocessor subsystem. The design of the InfoPad attempted to reduce the requirements of this general purpose processor by moving the computation into the network or by the use of highly optimized integrated circuits but in spite of these efforts it still was a major consumer of energy. The reasons for this became apparent as we determined that the energy required to perform a function in dedicated hardware could be several orders of magnitude lower than that consumed in the InfoPad microprocessor. We therefore set out on a full fledged attack on all aspects of the microprocessor energy consumption. 1 J After considerable analysis it became clear that though better circuit design and a stream lined architecture would assist in our goal of energy reduction that the biggest gains were to be found by operating at reduced voltages. For the busses and VO this could be accomplished without significant degradation of the processor performance but this was not a straightforward solution when applied to the core of the processor sub system CPU and memory.

**High-performance Energy-efficient Microprocessor Design** Vojin G. Oklobdzija, Ram K. Krishnamurthy, 2006  
**High-Performance Energy-Efficient Microprocessor Design** Vojin G. Oklobdzija, Ram K. Krishnamurthy, 2008-11-01 Written by the world's most prominent microprocessor design leaders from industry and academia this book provides complete coverage of all aspects of complex microprocessor design technology, power

management clocking high performance architecture design methodologies memory and I O design computer aided design testing and design for testability The chapters provide state of the art knowledge while including sufficient tutorial material to bring non experts up to speed A useful companion to design engineers working in related areas

**Energy Efficient High Performance Processors** Jawad Haj-Yahya, Avi Mendelson, Yosi Ben Asher, Anupam Chattopadhyay, 2018-03-22 This book explores energy efficiency techniques for high performance computing HPC systems using power management methods Adopting a step by step approach it describes power management flows algorithms and mechanism that are employed in modern processors such as Intel Sandy Bridge Haswell Skylake and other architectures e g ARM Further it includes practical examples and recent studies demonstrating how modern processors dynamically manage wide power ranges from a few milliwatts in the lowest idle power state to tens of watts in turbo state Moreover the book explains how thermal and power deliveries are managed in the context this huge power range The book also discusses the different metrics for energy efficiency presents several methods and applications of the power and energy estimation and shows how by using innovative power estimation methods and new algorithms modern processors are able to optimize metrics such as power energy and performance Different power estimation tools are presented including tools that break down the power consumption of modern processors at sub processor core thread granularity The book also investigates software firmware and hardware coordination methods of reducing power consumption for example a compiler assisted power management method to overcome power excursions Lastly it examines firmware algorithms for dynamic cache resizing and dynamic voltage and frequency scaling DVFS for memory sub systems

**Microprocessor Energy Characterization and Optimization Through Fast, Accurate, and Flexible Simulation** Ronny Meir Krashinsky, 2001

**Energy-Efficient Communication Processors** Robert Fasthuber, Francky Catthoor, Praveen Raghavan, Frederik Naessens, 2013-05-29 This book describes a new design approach for energy efficient Domain Specific Instruction set Processor DSIP architectures for the wireless baseband domain The innovative techniques presented enable co design of algorithms architectures and technology for efficient implementation of the most advanced technologies To demonstrate the feasibility of the author s design approach case studies are included for crucial functionality of advanced wireless systems with increased computational performance flexibility and reusability Designers using this approach will benefit from reduced development product costs and greater scalability to future process technology nodes

**Energy-efficient Processor System Design** Thomas David Burd, 2001

**Low-Power CMOS Design** Anantha Chandrakasan, Robert W. Brodersen, 1998-02-11 This collection of important papers provides a comprehensive overview of low power system design from component technologies and circuits to architecture system design and CAD techniques LOW POWER CMOS DESIGN summarizes the key low power contributions through papers written by experts in this evolving field

**Design of Energy-Efficient Application-Specific Instruction Set Processors** Tilman Glokler, Heinrich Meyr, 2014-01-15

**Energy-efficient Operating System Techniques** Trevor A.

Pering,2000     **High Performance and Energy Efficient Multi-core Systems for DSP Applications** Zhiyi Yu,2007  
Wireless Sensor Mote Processor Design Aiyappa Mandepanda,2008     **System-Level Design Techniques for Energy-Efficient Embedded Systems** Marcus T. Schmitz,Bashir M. Al-Hashimi,Petru Eles,2006-01-16 System Level Design Techniques for Energy Efficient Embedded Systems addresses the development and validation of co synthesis techniques that allow an effective design of embedded systems with low energy dissipation The book provides an overview of a system level co design flow illustrating through examples how system performance is influenced at various steps of the flow including allocation mapping and scheduling The book places special emphasis upon system level co synthesis techniques for architectures that contain voltage scalable processors which can dynamically trade off between computational performance and power consumption Throughout the book the introduced co synthesis techniques which target both single mode systems and emerging multi mode applications are applied to numerous benchmarks and real life examples including a realistic smart phone

**Design of High-Performance Microprocessor Circuits** Anantha Chandrakasan,2001 The authors present readers with a compelling one stop advanced system perspective on the intrinsic issues of digital system design This invaluable reference prepares readers to meet the emerging challenges of the device and circuit issues associated with deep submicron technology It incorporates future trends with practical contemporary methodologies     Parallel and Distributed Systems (ICPADS 2004) Nian-Feng Tzeng,2004 The proceedings of the July 2004 conference consists of 66 papers presenting recent research on peer to peer networks routing in optical networks caching and scheduling parallel algorithms grid and distributed systems wireless sensor networks performance evaluation and load balancing Three i     *Optimizing Processor Architectures for Power-efficiency* John Seng,2003     Modeling and Microarchitecture for Low Power Ravishankar V. Rao,2006     *High Performance Integrated Circuit Design* Emre Salman,Eby G. Friedman,2012-08-14 The latest techniques for designing robust high performance integrated circuits in nanoscale technologies Focusing on a new technological paradigm this practical guide describes the interconnect centric design methodologies that are now the major focus of nanoscale integrated circuits ICs High Performance Integrated Circuit Design begins by discussing the dominant role of on chip interconnects and provides an overview of technology scaling The book goes on to cover data signaling power management synchronization and substrate aware design Specific design constraints and methodologies unique to each type of interconnect are addressed This comprehensive volume also explains the design of specialized circuits such as tapered buffers and repeaters for data signaling voltage regulators for power management and phase locked loops for synchronization This is an invaluable resource for students researchers and engineers working in the area of high performance ICs Coverage includes Technology scaling Interconnect modeling and extraction Signal propagation and delay analysis Interconnect coupling noise Global signaling Power generation Power distribution networks CAD of power networks Techniques to reduce power supply noise Power dissipation Synchronization theory and tradeoffs Synchronous system

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